WHAT IS CLAIMED IS:

1. A memory circuit comprising:

a transistor whose gate is connected to input a data signal; and

first and second storage capacitances which are charged to positive and negative power supply voltages and connected to a source and drain of said transistor to store the data signal as analog drive voltages of positive and negative polarities, respectively.

2. The memory circuit according to claim 1, further comprising a switch circuit which initially connects said first and second storage capacitances to power lines of the positive and negative polarities which supply the positive and negative power supply voltages, respectively, and then connects said first and second storage capacitances to the source and drain of said transistor, respectively.

3. The memory circuit according to claim 2, further comprising an output circuit which outputs the analog drive voltages of the positive and negative polarities held by said first and second storage capacitances.

4. The memory circuit according to claim 1, wherein said transistor is one of P- and N-channel transistors.

5. The memory circuit according to claim 3, wherein said switch circuit includes a second

transistor connected between said power line of the positive polarity and said first storage capacitance, a third transistor connected between said power line of the negative polarity and said second storage capacitance, a fourth transistor connected between the source of said first transistor and said first storage capacitance, a fifth transistor connected between said the drain of said first transistor and said second storage capacitance, said second and third transistors are controlled to temporarily turn on for setting said first and second storage capacitances to the positive and negative power supply voltages, respectively, and said fourth and fifth transistors are controlled to temporarily turn on, in place of said second and third transistors, for causing said first and second storage capacitances to store the data signal as the analog drive voltages of the positive and negative polarities, respectively.

6. The memory circuit according to claim 5, wherein said output circuit includes sixth and seventh transistors whose gates are connected to said first and second storage capacitances, an eighth transistor connected at one end to said power line of the positive polarity via said sixth transistor and at the other end to a first load, and a ninth transistor connected at one end to said power line of the negative polarity via said seventh transistor and at the other end to

a second load, and conduction of said eighth and ninth transistors are controlled.

7. The memory circuit according to claim 6, wherein said first, third, fifth, seventh, and ninth transistors are P-channel transistors, and said second, fourth, sixth, and eighth transistors are N-channel transistors.

8. The memory circuit according to claim 7, wherein the threshold voltages of said P-channel and N-channel transistors differ from each other in absolute value, said switch circuit further includes a tenth transistor connected between said first storage capacitance and said fourth transistor, said output circuit includes an eleventh transistor connected between said sixth and eighth transistors and a twelfth transistor connected between said seventh and ninth transistors, said tenth, eleventh, twelfth transistors are N-channel, P-channel, and N-channel transistors serving as voltage drop elements which compensate for a difference in the threshold voltages to provide the drive voltages of the positive and negative polarities equal in absolute value.

9. The memory circuit according to claim 6, wherein said first and second loads are formed of a common liquid crystal display element having a structure that liquid crystal materials are held between a pair of electrodes.

10. A display circuit comprising:

a liquid crystal display element having a structure that liquid crystal materials are held between a pair of electrodes;

a memory circuit having a transistor whose gate is connected to input a data signal, and first and second storage capacitances which are charged to positive and negative power supply voltages and connected to a source and drain of said transistor to store the data signal as analog drive voltages of positive and negative polarities, respectively; and

an output circuit which alternately applies the analog drive voltages of the positive and negative polarities held by said first and second storage capacitances to said liquid crystal display element.

11. The display circuit according to claim 10, wherein said memory circuit includes a switch circuit which initially connects said first and second storage capacitances to power lines of the positive and negative polarities which supply the positive and negative power supply voltages, respectively, and then connects said first and second storage capacitances to the source and drain of said transistor, respectively.

12. A display device comprising:

a plurality of pixels arrayed in a matrix of rows and columns;

a plurality of scanning lines extending along the

rows of said pixels;

a plurality of signal lines extending along the columns of said pixels; and

a plurality of pixel driving sections which are disposed near intersections of said scanning and signal lines, and each of which is controlled via one scanning line to capture a data signal on one signal line and output the data signal to one pixel, each pixel driving section including a memory circuit having a transistor whose gate is connected to the one signal line, and first and second storage capacitances which are charged to positive and negative power supply voltages and connected to a source and drain of said transistor to store the data signal as analog drive voltages of positive and negative polarities, respectively.

13. The display device according to claim 12, wherein said memory circuit includes a switch circuit which initially connects said first and second storage capacitances to power lines of the positive and negative polarities which supply the positive and negative power supply voltages, respectively, and then connects said first and second storage capacitances to the source and drain of said transistor, respectively.

14. The display device according to claim 13, wherein said memory circuit further includes an output circuit which outputs the analog drive voltages of the positive and negative polarities held by said first and

second storage capacitances.

15. The display device according to claim 14, wherein said switch circuit includes a second transistor connected between said power line of the positive polarity and said first storage capacitance, a third transistor connected between said power line of the negative polarity and said second storage capacitance, a fourth transistor connected between the source of said first transistor and said first storage capacitance, a fifth transistor connected between said the drain of said first transistor and said second storage capacitance, said second and third transistors are controlled to temporarily turn on for setting said first and second storage capacitances to the positive and negative power supply voltages, respectively, and said fourth and fifth transistors are controlled to temporarily turn on, in place of said second and third transistors, for causing said first and second storage capacitances to store the data signal as the analog drive voltages of the positive and negative polarities, respectively.

16. The display device according to claim 15, wherein each of said scanning lines includes first subscanning lines of the positive and negative polarities which supply positive and negative pulses as a scanning signal to turn on said second and third transistors in one horizontal scanning period, and

second subscanning lines of the positive and negative polarities, which supply positive and negative pulses as the scanning signal to turn on said fourth and fifth transistors in one horizontal scanning period next to said horizontal scanning period.

17. The display device according to claim 16, wherein said second subscanning lines of the positive and negative polarities are common to said first subscanning lines of the positive and negative polarities for the pixels in a next row.

18. The display device according to claim 16, wherein said first subscanning lines of the positive and negative polarities are connected as ground lines to said first and second storage capacitances of each of the memory circuits for the pixels in a next row.

19. The display device according to claim 13, wherein said switch circuit includes a pulse shaping circuit which inverts a gate pulse applied to one of the gates of said second and third transistors and supplied the inverted gate pulse to the other one of the gates of said second and third transistors.

20. The display device according to claim 15, wherein said output circuit includes sixth and seventh transistors whose gates are connected to said first and second storage capacitances, an eighth transistor connected at one end to said power line of the positive polarity via said sixth transistor and at the other end

to a first load, and a ninth transistor connected at one end to said power line of the negative polarity via said seventh transistor and at the other end to a second load, and conduction of said eighth and ninth transistors are controlled.

21. The display device according to claim 20, wherein said first, third, fifth, seventh, and ninth transistors are P-channel transistors, and said second, fourth, sixth, and eighth transistors are N-channel transistors.

22. The display device according to claim 21, wherein the threshold voltages of said P-channel and N-channel transistors differ from each other in absolute value, said switch circuit further includes a tenth transistor connected between said first storage capacitance and said fourth transistor, said output circuit includes an eleventh transistor connected between said sixth and eighth transistors and a twelfth transistor connected between said seventh and ninth transistors, said tenth, eleventh, twelfth transistors are N-channel, P-channel, and N-channel transistors serving as voltage drop elements which compensate for a difference in the threshold voltages to provide the drive voltages of the positive and negative polarities equal in absolute value.

23. The display device according to claim 20, wherein each of said pixels has a structure that liquid

crystal materials are held between a pair of electrodes, and said first and second loads are formed of a common one of said pixels.